

CLEAN VERSION OF AMENDED SPECIFICATION PARAGRAPHS

**PIPELINED PACKET-ORIENTED MEMORY SYSTEM HAVING A UNIDIRECTIONAL
COMMAND AND ADDRESS BUS AND A BIDIRECTIONAL DATA BUS**

Applicant: Kevin J. Ryan

Serial No.: 09/434,082

Paragraph beginning at page 8, line 3:

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~~— Each memory subsystem 130 includes a C/A buffer register 131, a plurality M of memory devices 135 and a data buffer register 141. C/A buffer register 131 receives and latches the command and address information from C/A bus 110. As illustrated in Figure 1, buffer register 131 is connected between the command and address bus 110 and the plurality of memory devices 135.1 through 135.M. In one embodiment, memory system 100 has eight memory subsystems and eight memory devices 135 (i.e. N plus M equals sixteen). In another embodiment, memory devices 135 are dynamic random access memory devices (DRAMs). The number of memory devices 135 connected to each buffer register 131 may, however, differ from that shown in memory system 100 without departing from the spirit of the present invention.~~ *DA*